CLAIMS:

1. (Canceled)

2. (Previously presented) The semiconductor apparatus as set forth in claim 25, wherein the surfaces of the metal bumps projecting out from the resin film are cleaned of components causing a rise of a connection resistance and a drop in a joint strength at least at connection interfaces.

3-5. (Canceled)

6. (Previously presented) The semiconductor apparatus as set forth in claim 25, wherein said solder bumps are comprised of high metal point solder and said solder layers are comprised of a eutectic solder.

7-24. (Canceled)

25. (Previously presented) A semiconductor apparatus comprising:

a semiconductor chip having a circuit pattern disposed thereon;

a plurality of solder bumps formed on said semiconductor chip and connecting to said circuit pattern, said solder bumps forming spaces therebetween;

a resin film disposed on said semiconductor chip and directly contacting said solder bumps, said resin film being disposed in the spaces between solder bumps such that upper surfaces of said solder bumps protrude from said resin layer;

wherein said upper surfaces of said solder bumps are cleaned of impurities;

a eutectic solder layer disposed on said cleaned upper surfaces of said solder bumps;

a mounting board;

a plurality of lands formed on said mounting board and aligned opposite said solder bumps; and

a precoated solder layer disposed on said lands;

wherein said eutectic solder layer of said solder bumps and said precoated solder layer join said upper surfaces of said solder bumps to said lands of said mounting board such that a stacked structure is obtained;

wherein a gap is formed between said resin layer and said mounting board of said stacked structure.

26. (Previously presented) The semiconductor apparatus as set forth in claim 25, wherein said eutectic solder layer of said solder bumps and said precoated solder layer intermix to join said upper surfaces of said solder bumps to said lands of said mounting board.

27. (Previously presented) The semiconductor apparatus as set forth in claim 25, wherein said resin film includes an epoxy-based resin film cured at about 150°C for about 5 hours after being spin-coated in place.

28. (Previously presented) The semiconductor apparatus as set forth in claim 25, wherein said upper surfaces of said solder bumps are plasma cleaned of impurities.

29. (Previously presented) The semiconductor apparatus as set forth in claim 25, wherein said precoated solder layer comprises a eutectic solder.

30. (Previously presented) The semiconductor apparatus as set forth in claim 25, wherein each of said lands has a top side, a bottom side opposite said top side and directly contacting the mounting board, and side walls extending from the top side to the bottom side.

31. (Previously presented) The semiconductor apparatus as set forth in claim 25, wherein said mounting board includes an upper surface, the upper surface having land portions on which said lands are formed.

32. (Previously presented) The semiconductor apparatus as set forth in claim 31, further comprising solder resists formed on the mounting board intermediate adjacent lands of the plurality of lands.